**Course Name: Computer Architecture**

**Course Code: BCA115A**

|  |  |  |  |
| --- | --- | --- | --- |
| **L (Hr.)** | **T (Hr.)** | **Pr (Hr.)** | **Credits** |
| 3 | 1 | 0 | 4 |

**Course Objectives:-**

1. To provide information about digital computer technology and computer system performance.
2. To describe concepts of instruction-set architecture.
3. To clear concepts of central processing unit and describes the structure of arithmetic/logic units.
4. To have a systematic understanding of the basic structure and operation of a digital computer.
5. To discuss in detail the operation of the arithmetic Unit including the algorithms & implementation of fixed-point and floating-point addition, subtraction, multiplication & division.

**Syllabus**

**Unit I**

**Background And Motivation:** Combinational Digital Circuits, Signals, Logic Operators, and Gates, Boolean Functions and Expressions, Designing Gate Networks, Useful Combinational Parts, Programmable Combinational Parts, Timing and Circuit Considerations

Digital Circuits with Memory: Latches, Flip-Flops, and Registers, Finite-State Machines, Designing Sequential Circuits

**Unit II**

**Computer System Technology & Performance:** From Components to Applications, Computer Systems and Their Parts, Generations of Progress, Processor and Memory Technologies, Peripherals, I/O, and Communications, Software Systems and Applications

Computer Performance: Cost, Performance, and Cost/Performance, Defining Computer Performance, Performance Measurement vs. Modeling Reporting Computer Performance, The Quest for Higher Performance

**Unit III**

**Instruction-Set Architecture**: Instructions and Addressing: Abstract View of Hardware, Instruction Formats, Simple Arithmetic and Logic Instructions, Load and Store Instructions, Jump and Branch Instructions, Addressing Modes.

Procedures and Data: Simple Procedure Calls, Using the Stack for Data Storage, Parameters and Results, Data Types, Arrays and Pointers, Additional Instructions

**Unit IV**

**Arithmetic/Logic Unit:** Number Representation: Positional Number Systems, Digit Sets and Encodings, Number-Radix Conversion, Signed Integers, Fixed-Point Numbers, Floating-Point Numbers.

Adders and Simple ALUs: Simple Adders, Carry Propagation Networks, Counting and Instrumentation, Design of Fast Adders, Logic and Shift Operations.

Multipliers and Dividers: Shift-Add Multiplication, Hardware Multipliers, Programmed Multiplication, Shift-Subtract Division, Hardware Dividers, Programmed Division.

**Unit V**

**Memory System Design:** Main Memory Concepts: Memory Structure and SRAM, DRAM and Refresh Cycles, Hitting the Memory Wall, Pipelined and Interleaved Memory, Nonvolatile Memory, Need for a Memory Hierarchy.

Cache Memory Organization: The Need for a Cache, Direct-Mapped Cache, Set-Associative Cache, Cache and main Memory, improving Cache Performance.

**Course Outcomes (COs):-**

**On successful completion of this course, the learner will be able to**

CO1: Students are able to understand concept of combination and digital circuits.

CO2: Able to understand Computer systems and Computer Performance.

CO3: To describe Instruction set Architecture, Simple Procedure Calls.

CO4: Able to understand ALU functioning and Architecture, Multipliers and Dividers.

CO5: Enhance the knowledge of Memory system design, cache memory organization and interleaved memory.

**Reference Books :**

* + - 1. Carl Hamacher, ZvonkoVranesic and SafwatZaky, Naraig Manjikian, “Computer Organization and Embedded Systems”,(6e),McGraw Hill Publication, 2012
      2. D. A. Patterson and J. L. Hennessy, “Computer Organization and Design - The Hardware/Software Interface”,(5e),Morgan Kaufmann, 2011
      3. Mohammed Rafiquzzaman and Rajan Chandra, “Modern Computer Architecture”, Galgotia Publications Pvt. Ltd. 2008.
      4. William Stallings, “Computer Organization and Architecture Designing for Performance”, (8e), PHI, 2009.